Application Serial No. 10/584,778   PATENT
Reply to final office action of March 4, 2010   Docket: CU-4906

Remarks and Arguments

Upon entry of the foregoing amendments, claims 1, 3, 6 and 7 will remain pending in the application. Claims 1, 3, 6 and 7 have been amended. The amendments are supported by the context of the claims and FIGs. 2-4 as well as the corresponding written description in the specification, and do not introduce new matter. Their entry is therefore respectfully requested.

In the Office Action of March 4, 2009, the examiner set forth a number of grounds for rejection. These grounds are addressed individually and in detail below.

Claim Rejections Under 35 U.S.C. §112

In the office action (page 2), the examiner objects to claim 1 for containing informalities.

In the office action (page 2), claim 1 stands rejected under 35 U.S.C. §112, ¶1, as being unclear for the reasons set forth in Items 3 and 6 of the Office Action.

The applicant has amended claim 1 to address the examiner's concerns.

In the office action (page 3), the examiner rejects claim 3 under 35 U.S.C. § 112, ¶1, as failing to comply with the written description requirement and being indefinite for the reasons set forth in Items 4 and 7.

The applicant has cancelled the recitations in question from claim 3 thereby rendering the rejection of claim 3 moot.

In the office action (page 4), the examiner rejects claim 7 under 35 U.S.C. § 112, ¶2, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The applicant has amended claim 7 according to the examiner's suggestions.

Claim Rejections Under 35 U.S.C. §102

In the office action (page 5), claims 1, 3, 6 and 7 stand rejected under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent No. 5,671,439 (Klein et al.).

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     Independent claim 1 of the present application, as amended, is directed to a data write-in method for a flash memory, wherein the flash memory comprises at least two flash chips and a controller, and the method comprises: partitioning physical blocks in the flash chips to odd logical block addresses and even logical block addresses, respectively; the controller receiving a data write-in instructions and analyzing a beginning logical address for writing from the received data write-in instruction; the controller obtaining the logical block address needed to be written according to the analyzed beginning logical address; the controller determining a parity of the obtained logical block address, and selecting one flash chip from the flash chips according to the determined parity of the logical block address; the controller directing a first programming or erasing instruction to the physical blocks corresponding to the obtained logical block address in the selected flash chip; the controller detecting whether the other flash chip needs to be programmed or erased while the first programming or erasing instruction are being processed; if programming or erasing is needed in the other flash chip the method further comprises: the controller directing a second programming or erasing instruction to the other flash chip of at least two flash chips.

     Accordingly to the claim 1 of the subject application, as amended, the first and second programming or erasing instructions are sent to at least two flash chips by the controller **arranged in the flash memory.** While a first flash chip of the at least two flash chips is processing the first programming or erasing instruction, the controller detects and sends the second programming or erasing instruction to the other flash chip (which is also arranged in the flash memory) to process the second programming or erasing instruction. Accordingly, the flash memory (in particular, the controller of the flash memory) may communicate with a host that sends the first and second programming or erasing instructions **through a single data channel** to the controller.

     However, *Klein et al* fails to disclose flash chips. The solution disclosed by *Klein et al* are applicable to conventional storage devices like hard disk drives, optical drives and tape back drivers, etc.. Please refer to Lines 24-25 of Column 1 of *Klein et al*. A drive controller in the host sends operating instructions to the storage devices via **an IDE interface circuit, SCSI bus or PCI bus**. Please refer to Lines 6-7 of Column 2 of

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Klein et al and FIGs. 6 and 7. Accordingly, although sectors of logical addresses of the virtual devices of *Klein et al* may be allocated between two physical devices (drive A and drive B) using block-by-block interleaving, the drive controller in the host needs separate data channels to communicate with the drive A or Drive B. That is, **two separate data channels** between the host and the storage devices are needed.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *Scripps Clinic Research & Foundation v. Genentech Inc.*, 18 USPQ2d 1001, 1010 (Fed. Cir. 1991).

As discussed above, *Klein et al* at least fails to disclose all of the features of the amended claim 1 of the application, and thus claim 1 is not anticipated by *Klein et al*.

Accordingly, claims 3, 6, and 7 are not anticipated by *Klein et al*, as they depend on claim 1 and recite all the limitations of claim 1. Withdrawal of the rejection of claims under 35 U.S.C. §102 is respectfully requested.

NO DISCLAIMERS OR DISAVOWALS

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the applicant is not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. The applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that the Applicants have made any disclaimers or disavowals of any subject matter

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supported by the present application.

Conclusion

For the reasons set forth above, the applicant respectfully submits that claims 1, 3, 6 and 7 pending in this application are in condition for allowance over the cited references. Accordingly, the applicant respectfully requests reconsideration and withdrawal of the outstanding rejections and earnestly solicits an indication of allowable subject matter.

This amendment is considered to be responsive to all points raised in the office action. Should the examiner have any remaining questions or concerns, the examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

Dated: _May 28, 2010_
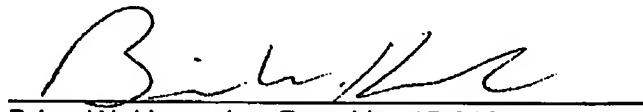
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